THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 41

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte NANETTE BROWN

Appeal No. 95-1955
Application 08/109,982[1]

ON BRIEF

Before URYNOWICZ, KRASS and LEE, Administrative Patent Judges.

LEE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 10-12, all of which are independent claims. No claim has been allowed.

Reference Relied on by the Examiner

Nibby, Jr. et al. Patent No. 4,527,251 Jul. 2, 1985
(Nibby)

Application for patent filed August 23, 1993. According to the appellant, it is a continuation application of application 07/827,911, filed on January 31, 1992, now abandoned, which is a continuation application of application 07/292,195, filed on December 30, 1988, also now abandoned.

Hills et al. (Hills) Patent No. 4,713,769 Dec. 15, 1987

The Rejection on Appeal

Claims 10-12 stand rejected under 35 U.S.C. § 112, first paragraph, as being based on new matter added to the disclosure subsequent to the filing of the application. We regard the rejection as being for lack of adequate written description in the specification as is required by § 112, first paragraph.

Claims 10-12 stand rejected under 35 U.S.C. § 112, second paragraph, as failing to particularly point out what the appellant regard as her invention.

Claims 10-12 also stand rejected under 35 U.S.C. § 103 as being unpatentable over Nibby and Hills.

The Invention

The invention is directed to a method for organizing data in a postage meter microcontrol system. Claim 10 is representative and reads as follows:

> 10. A method for organizing data in a postage meter microcontrol system, said postage meter microcontrol system having a plurality of non-volatile memory, a CPU and a Read Only Memory (ROM) comprising the steps of:
>
> (a) allocating a plurality of data stores for a first one of said non-volatile memories, each data store having a plurality of buffers, said plurality of buffers containing related data items;

(b) allocating a plurality of data stores for a second one of said non-volatile memories, each data store having a plurality of buffers containing redundant data to a respective one of said buffers in said first one of said non-volatile memory;

(c) providing a data store in each of said non-volatile memories which data store includes a bit map buffer having first data therein relating to the status of each of a plurality of buffers of said respective non-volatile memory and said respective bit map buffers includes status data only for that respective non-volatile memory wherein said first data has a first state and a second state;

(d) providing and entry table of addresses in said ROM for accessing the data store in each of said respective non-volatile memories;

(e) determining a current buffer address for accessing said respective non-volatile memories in accordance with the data in said ROM table and said non-volatile memory bit map;

(f) calculating and storing an associated CRC for only those data stores having said respective first data in a first state in each of said buffers of said respective non-volatile memories wherein said CRC has a first state representing a good data store buffer and a second state representing a bad data store buffer;

(g) setting said first data to said first state when said CRC is in a first state or to said second state when said CRC is in said [second] state; [and],

(h) programing said microcontrol system to access only those data stores wherein said first data is in said first state.

Note that claims 11 and 12 do not require that the second non-volatile memory contain redundant data with respect to the buffers in the data stores of the first non-volatile memory.

Note also that claim 12's steps (g) and (h) appear to be duplicative to each other. The appellant or the examiner may want to take up this matter upon return of the application to the examining group upon termination of this appeal.

Opinion

The appellant's reply brief (Paper No. 37) was not entered by the examiner (See Paper No. 38). Therefore, it is not a part of the record in this appeal and has not been considered.

The rejection under 35 U.S.C. § 112, first paragraph

We do not sustain the rejection of claims 10-12 under 35 U.S.C. § 112, first paragraph, as being without adequate written description support in the specification.

Claim 10 recites the step of "calculating and storing an associated CRC for only those data stores having said respective first data in a first state in each of said buffers of said respective non-volatile memories wherein said CRC has a first state representing a good data store buffer and a second state representing a bad data store buffer." Essentially the same feature is recited in claims 11 and 12 as well. The acronym "CRC" is defined on page 8 of the specification and it means "cyclic redundancy code."

According to the claimed invention, the CRC is not

calculated and stored for every data store in the non-volatile memories, but only for those stores whose corresponding first data in the bit map buffer is in a first state. The claimed invention includes a bit map buffer in one of the data stores of each non-volatile memory, which has first data therein relating to the status of each buffer in the associated non-volatile memory. The first data has a first state and a second state.

In the specification, evidently the only place where the generation of CRC is explicitly discussed is on page 8:

> For best results, each data buffer will have an attached cyclic redundancy code (CRC) calculated. A single CRC is computed across all of the data items within the buffer. If the buffer contains unused space, the CRC calculation does not include such unused bytes. It will be appreciated that the calculation of a single CRC for the entire buffer will save considerable space over that required for CRC's for each data item. (Emphasis added.)

The examiner correctly notes that the above-quoted language uses the word "each" to describe which data store will have its CRC calculated. For reasons discussed below, we agree with the appellant that the specification as filed does have written description support for calculating and storing the CRC only for the good data buffers and not the buffers already marked bad. The rejection of claims 10-12 under 35 U.S.C. § 112, first paragraph, is erroneous.

The function of the description requirement is to ensure that the inventor had possession, as of the filing date of the application relied on, of the specific subject matter later claimed by him. In re Wertheim, 541 F.2d 257, 265, 191 USPQ 90, 98 (CCPA 1976). How the specification accomplishes this is not material, and it is not necessary that the specification describe the claim limitations exactly. Id. Under the written description requirement, a specification need not describe the claimed invention in ipsis verbis to comply with 35 U.S.C. § 112, first paragraph. In re Edwards, 568 F.2d 1349, 1351-52, 196 USPQ 465, 467 (CCPA 1978). The test is whether the originally filed specification reasonably conveys to a person having ordinary skill that applicant had possession of the subject matter later claimed. In re Kaslow, 707 F.2d 1366, 1375, 217 USPQ 1089, 1096 (Fed. Cir. 1983). Here, we think it does.

The examiner may not limit a review of the specification to only a single paragraph in the disclosure. Rather, the entire document must be considered as a whole in determining what it would convey to one with ordinary skill in the art. In that regard, we note several other portions of the specification:

Page 1, lines 24-32

> Random events may cause data within non-volatile memories to be incorrectly read or written. In postage

> meter operation, it is extremely important that such events be detected and the READ or WRITE operation be retried. If the incorrect READ or WRITE is determined to be a result of a problem with the memory device, the data must be reconstructed, for instance in the case of a failed read, and then relocated to a different part of the non-volatile memory.
>
> Page 2, lines 10-13
>
> Also, as brought out in the teaching of [another] application, each data item stored in the block requires its own CRC for determination of whether the register data is corrupt.

The foregoing sets up the context in which memory fault corruptions are detected or determined as a part of each memory READ and WRITE operation, and in which corruption is determined on the basis of calculating the corresponding CRC.

As is described on page 15 and shown in the flow chart on Figure 10A, the READ is "tested" at decision block 1280, after the READ operation takes place in block 1270. Similarly, as is described on page 17 and shown in the flow chart in Figure 11, the WRITE is tested at decision block 1470, after the WRITE operation takes place in block 1450. One with ordinary skill in the art would understand that the testing referred to concerns the detection of memory fault or corruption and thus relates to the generation of the CRC. Evidently, the appellant argues the same. (Br. page 6, line 30 to page 7, line 2).

Figure 10A reveals that the READ operation is not performed

for those buffers which have already been marked bad (box 1260). Figure 11 reveals that the WRITE operation is not performed for those buffers which have already been marked bad (box 1440). Figure 10A indicates that if there is no READING, there is no corresponding testing for READING (box 1280). See also the description on page 15 of the specification. Similarly, Figure 11 indicates that if there is no WRITING, there is no corresponding testing for WRITING (box 1470). See also the description on pages 16-17 of the specification. Given that the testing referred to involves the generation of the CRC, the specification as filed does have adequate written description support for generating and storing the CRC only for the good buffers. The good buffers, in that regard, are those whose corresponding first data in the bit map buffer have been set to a first state as opposed to a second state.

In our view, the examiner failed to address and explain the implication and significance of other description in the specification tending to support the appellant's position, and merely focused on a single paragraph of text to the exclusion of other relevant evidence. Upon consideration of the entirety of the specification as a whole, and as discussed above, we find that the rejection of claims 10-12 under 35 U.S.C. § 112, first

paragraph, as lacking adequate written description support in the specification is without merit.

Accordingly, the rejection of claims 10-12 under 35 U.S.C. § 112, first paragraph, as being without adequate written description support in the specification cannot be sustained.

The rejection under
35 U.S.C. § 112, second paragraph

We do not sustain the rejection of claims 10-12 under 35 U.S.C. § 112, second paragraph, as being indefinite or failing to particularly point out and distinctly claim that subject matter which the applicant regards as her invention.

The test for compliance with 35 U.S.C. § 112, second paragraph, is:

> [W]hether the claim language, when read by a person of ordinary skill in the art in light of the specification, describes the subject matter with sufficient precision that the bounds of the claimed subject matter are distinct. In re Merat, 519 F.2d 1390, 1396, 186 USPQ 471, 476 (CCPA 1975).

The purpose of the statutory section is to provide reasonable notice as to the boundaries of the patent protection involved. In re Hammack, 427 F.2d 1378, 1382, 166 USPQ 204, 208 (CCPA 1970). Only a reasonable degree of certainty is required.

In re Johnson, 558 F.2d 1008, 1016, 194 USPQ 187, 194 (CCPA 1977).

The only reason articulated by the examiner in support of the indefiniteness rejection under 35 U.S.C. § 112, second paragraph, is that the claims as recited are without adequate written description in the specification under 35 U.S.C. § 112, first paragraph. See examiner's answer at page 3.

Even assuming that the claims are without written description support in the specification, that does not establish that the appellant has failed to particularly point out the subject matter which she regards as the invention. The examiner does not assert and has no reasonable basis to assert that one with ordinary skill in the art, upon reading the claims, would not know the scope of the claimed invention or what has been claimed. The written description requirement of 35 U.S.C. § 112, first paragraph, and the definiteness requirement of 35 U.S.C. § 112, second paragraph, have entirely different purposes and are independent of each other. In any event, we have also found above that the rejection of claims 10-12 under 35 U.S.C. § 112, first paragraph, as being without adequate written description support in the specification cannot be sustained.

Accordingly, we do not sustain the rejection of claims 10-12

under 35 U.S.C. § 112, second paragraph.

The rejection of claims 10-12 as
being obvious under 35 U.S.C. § 103

We do not sustain the rejection of claims 10-12 under 35 U.S.C. § 103 as being unpatentable over Nibby and Hill.

The examiner found as follows (answer at 3):

> To test a data store's memory segment, Nibby, Jr. et al's method performs a test on each storage location associated with each addressable location of the memory segment. After each addressable location in a memory segment has been tested, the results of these tests is used to determine whether or not the entire segment of the data store is good or bad. If the memory segment of the data store contains at least one bad addressable location, then that entire segment of the data store is marked as bad. Otherwise that segment of the data store is marked as good. The results of this determination is then used to create a bit map buffer, which inherently has two states, i.e., a state representing a good area and the alternative state representing a bad area.

None of the foregoing is disputed by the appellant. However, two issues are in apparent dispute. First, the claimed invention requires that the bit map buffer be contained in a data store of a non-volatile memory. Secondly, the claimed invention recites that the cyclic redundancy code CRC is calculated only for those data stores whose corresponding first data in the bit map are in a first state and not for all data stores.

The appellant correctly asserts (Br. at 11-12) that Nibby puts its bit map in a static RAM which is a volatile memory,

whereas the claimed invention requires a non-volatile memory for storing the bit map. The appellant further explains (Br. at 11) the significance of putting the bit map in a non-volatile memory in noting that it becomes unnecessary to reconstruct the bit map during each subsequent power up and it is only necessary to test those segments previously tested as good during the last write cycle to that address. The non-volatile memory feature is a substantial and meaningful feature of the claimed invention. Also, the claims recite that the cyclic redundancy code CRC is calculated only for those data stores whose corresponding first data in the bit map are in a first rather than a second state.

In stating the rejection (answer at 3), the examiner did not explain where in Nibby is the disclosure or suggestion for storing the bit map in a non-volatile memory. Even if Nibby's ROM which is a non-volatile memory stores the starting addresses of the bit map or other data stores, the bit map itself with first data having either a first state or a second state is stored in a volatile memory (column 3, lines 11-15 and 40-52). In responding to the appellant's argument, the examiner erroneously states (answer at 8, ¶ 10): "appellant agrees that Nibby, Jr. et al uses a ROM (I.E., A NON-VOLATILE MEMORY) to store a bit map to [indicate] which buffer sections of a memory

are either good or bad." We do not see that the appellant has made any such representation. The appellant consistently asserted that in Nibby, the bit map is stored in a volatile memory. (Br. at 11, line 23 and at 12, lines 3-8). Indeed, the appellant stated (Br. at 12, lines 7-10):

> Appellant places the bit map for the respective nonvolatile memories in a portion of the respective nonvolatile memory. Therefore, it is unnecessary to remap the respective memories during power-up. It is only necessary to check the previously marked memory area designated as good.

The examiner also has not pointed to anything in Nibby and we have not located any teaching in Nibby which reasonably suggests doing a memory check, whether by calculating the CRC or by any other method, only for those data stores whose first data in the bit map are in a first rather than a second state. Each of the appealed claims includes that feature in the form of calculating and storing a CRC.

Hill has been relied on by the examiner in connection with that feature of the claimed invention which requires a second non-volatile memory containing redundant data to that stored in the first non-volatile memory. In the manner as applied by the examiner, Hill does not make up for the deficiencies of Nibby as discussed above.

It should be noted that the mere fact that the prior art may

be modified in the manner as suggested by the examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992). Here, the examiner has demonstrated no such suggestion stemming from the prior art.

For the foregoing reasons, the rejection of claims 10-12 under 35 U.S.C. § 103 as being unpatentable over Nibby and Hill cannot be sustained.

Conclusion

The rejection of claims 10-12 under 35 U.S.C. § 112, first paragraph, as being without adequate written description support in the specification is reversed.

The rejection of claims 10-12 under 35 U.S.C. § 112, second paragraph, as being indefinite or failing to particularly point out and distinctly claim that subject matter which the applicant regards as her invention is reversed.

The rejection of claims 10-12 under 35 U.S.C. § 103 as being unpatentable over Nibby and Hill is reversed.

REVERSED

STANLEY M. URYNOWICZ Administrative Patent Judge	)	
ERROL A. KRASS Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
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